

scope which significantly varies the scope and subject matter of the claims. Specifically, the claims recite different subject matter.

For example, independent claim 59 is directed to an asynchronous random access memory circuit. Claims 22-32 are not so limited. In fact, only claim 32 is directed to an asynchronous memory. The doctrine of claim differentiation precludes the reading into claim 22 of the limitation contained in claim 32 which is indirectly dependent on claim 22. Claim 32 depends on claim 26, which includes a counter not present in claim 59. As such, the subject matter of claim 59 is significantly different from that of claim 22.

Independent claims 60 and 61 define the mode control signal as being an external or an internal mode control signal. Each of the claims is significantly narrower than claim 22. The doctrine of claim differentiation precludes the limitation of external and internal mode control signals because of the limitations of claim 23. As such, the subject matter of claims 60-61 is significantly different from that of claims 22-32.

Independent claim 63 includes a second multiplexer for receiving the second external address. No such second multiplexer is present in claims 22-32, and as such the subject matter of claim 63 significantly differs from claims 22-32. Claim 64 depends from and further defines patentably distinct claim 62.

Independent claim 65 includes a counter coupled to receive first and second external addresses, and a pair of multiplexers, which are not contained in or recited in claims 22-32. As such, the scope of claim 65 clearly differs from that of claims 22-32.

### **§103 Rejection of the Claims**

Claims 22-32 and 59-65 were rejected under 35 USC § 103(a) as being unpatentable over Manning (U.S. Patent No. 5,610,864) in view of Ryan (U.S. Patent No. 5,966,724). Applicant traverses the rejections, and submits that the rejection fails to satisfy the prima facie case of obviousness, and as such, the rejections are improper and should be withdrawn.

Applicant continues to dispute that Manning shows a pipelined mode of operation. Ryan discusses only a synchronous burst access memory device, as is clear from a reading of the Ryan disclosure. Within the Ryan burst memory device, certain addresses can be received in a pipeline method. However, Ryan does not switch between a burst and a pipelined mode of operation.

Instead, within a burst operation, pipelined addresses may be received. In fact, Applicant can find no reference in col. 4, ll. 21-26, or for that matter in the entire Ryan specification, of any switching between burst and pipelined modes of operation. Instead, as has been mentioned, the memory device of Ryan is a synchronous burst access memory device.

Applicant submits that there is no motivation to combine Manning and Ryan. Switching between burst and pipelined modes of operation is not suggested in either Ryan, Manning, or any combination thereof. As has been discussed, no actual switching between burst and pipelines modes of operation is discussed in Ryan. Instead, within a burst mode, pipelined addresses may be received. This is fundamentally different from switching between burst and pipelined modes of operation. As no mention has been made in either reference of switching between burst and pipelined modes of operation, such a combination does not include the switching. Further, combination of the references does not result in both burst and pipelined modes of operation. Instead, as has been mentioned before in earlier arguments, which are incorporated herein again, it is only hindsight gained from Applicant's disclosure which suggests having both burst and pipelined modes of operation in a memory, and switching therebetween.

Manning and Ryan are further not properly combinable as Manning is directed to asynchronous memories and Ryan to synchronous memories. It is a specific unaddressed problem of asynchronous DRAMs to switch between burst and pipelined modes of operation since it was not previously needed. See the background of the invention, page 5, ll. 16-22.

With respect to claim 61, in addition to the discussion of Manning and Ryan above, the office action does not even assert that either Ryan or Manning, or any combination thereof, disclose providing an internal mode control signal. Instead, the only assertion of the office action is an external mode control signal.

With respect to claim 63, Applicant submits that Ryan clearly states that reference 18 is a latch, and reference 26 is a counter or latch. Latches and counters are not multiplexers. As such, Applicant submits that Ryan does not disclose first and second multiplexers as recited in claim 63.

The office action has not stated any specific grounds of rejection of claims 64 and 65. As such, the office action does not provide Applicant with sufficient detail to even understand the rejection of claims 64 and 65. As the office action has not shown how Manning, Ryan, or any

AMENDMENT AND RESPONSE

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combination thereof teaches or suggests the subject matter of claims 64 and 65, the rejection has not been supported. No specific mention of the elements of claims 64 and 65 is shown. Such a blanket recitation of elements without pointing out where the elements occur in the specification does not give Applicant the ability to properly understand the rejection. As such, Applicant asks that the specific elements of the claims be pointed out in Ryan, including specifically the location in the Ryan reference of such elements.

**CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.


If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

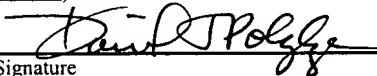
By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 373-6944

Date 10 March 2000 By   
Daniel J. Polglaze  
Reg. No. 39,801

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on March 10, 2000.

DANIEL J. POLGLAZE  
Name

  
Signature